

DIGITAL SIGNAL PROCESSING APPLICATIONS
USING THE ADSP-2100 FAMILY

ANALOG DEVICES TECHNICAL REFERENCE BOOKS

Published by Prentice Hall

Analog-Digital Conversion Handbook

Digital Signal Processing in VLSI

Digital Signal Processing Applications Using the ADSP-2100 Family

Published by Analog Devices

Nonlinear Circuits Handbook

Transducer Interfacing Handbook

Synchro & Resolver Conversion

DIGITAL SIGNAL PROCESSING APPLICATIONS
USING THE ADSP-2100 FAMILY

by

The Applications Engineering Staff of Analog Devices, DSP Division.

Edited by Amy Mar

PH logo here

PRENTICE HALL, Englewood Cliffs, NJ 07632

© 1990 by Analog Devices, Inc., Norwood, MA 02062

Prentice
Hall
logo here

Published by Prentice-Hall, Inc.
A Division of Simon & Schuster
Englewood Cliffs, New Jersey 07632

All rights reserved. No part of this book may be reproduced, in any form or by any means, without permission in writing from the copyright owner.

Information furnished by Analog Devices, Inc., is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices, Inc., for its use.

Analog Devices, Inc., makes no representation that the interconnection of its circuits as described herein will not infringe on existing or future patent rights, nor do the descriptions contained herein imply the granting of licenses to make, use, or sell equipment constructed in accordance therewith.

Specifications and prices are subject to change without notice.

Printed in the United States of America

10 9 8 7 6 5 4 3 2 1

ISBN

Prentice-Hall International (UK) Limited, *London*
Prentice-Hall of Australia Pty. Limited, *Sydney*
Prentice-Hall Canada Inc., *Toronto*
Prentice-Hall Hispanoamericana, S.A., *Mexico*
Prentice-Hall of India Private Limited, *New Delhi*
Prentice-Hall of Japan, Inc., *Tokyo*
Simon & Schuster Asia Pte. Ltd., *Singapore*

Table of Contents

	Page
Contents	v
Preface	
 CHAPTER 1 INTRODUCTION	
1.1 OVERVIEW	1
1.2 ADSP-2100 FAMILY OF PROCESSORS.....	1
1.2.1 ADSP-2100 Architecture.....	2
1.2.2 ADSP-2101 Architecture.....	6
1.3 ASSEMBLY LANGUAGE OVERVIEW.....	8
1.4 DEVELOPMENT SYSTEM.....	10
1.5 CONVENTIONS OF NOTATION.....	11
1.6 PROGRAMS ON DISK.....	12
1.7 FOR FURTHER SUPPORT.....	12
 CHAPTER 2 FIXED-POINT ARITHMETIC	
2.1 OVERVIEW	13
2.2 SINGLE-PRECISION FIXED-POINT DIVISION.....	15
2.3 MULTIPRECISION FIXED-POINT ADDITION.....	18
2.4 MULTIPRECISION FIXED-POINT SUBTRACTION.....	21
2.5 MULTIPRECISION FIXED-POINT MULTIPLICATION.....	23
2.6 MULTIPRECISION FIXED-POINT DIVISION.....	29
2.7 REFERENCES	31
 CHAPTER 3 FLOATING-POINT ARITHMETIC	
3.1 OVERVIEW	33
3.2 FIXED-POINT TO FLOATING-POINT CONVERSION.....	34
3.2.1 Fixed-Point (1.15) to IEEE Floating-Point.....	35
3.2.2 Fixed-Point (1.15) to Two-Word Floating-Point.....	36
3.3 FLOATING-POINT TO FIXED-POINT CONVERSION.....	37

3.3.1 IEEE Format to Fixed-Point Format (1.15).....	37
3.3.2 Two-Word Format to Fixed-Point Format (1.15).....	41
3.4 FLOATING-POINT ADDITION.....	42
3.5 FLOATING-POINT SUBTRACTION.....	43
3.6 FLOATING-POINT MULTIPLICATION.....	45
3.7 FLOATING-POINT DIVISION.....	47
3.8 FLOATING-POINT MULTIPLY/ACCUMULATE.....	48
3.9 REFERENCES	50

CHAPTER 4 FUNCTION APPROXIMATION

4.1 OVERVIEW	51
4.2 SINE APPROXIMATION.....	51
4.3 ARCTANGENT APPROXIMATION.....	54
4.4 SQUARE ROOT APPROXIMATION.....	57
4.5 LOGARITHM APPROXIMATION.....	61
4.6 UNIFORM RANDOM NUMBER GENERATION.....	64
4.7 REFERENCES	66

CHAPTER 5 DIGITAL FILTERS

5.1 OVERVIEW	67
5.2 FINITE IMPULSE RESPONSE (FIR) FILTERS.....	67
5.2.1 Single-Precision FIR Transversal Filter.....	68
5.2.2 Double-Precision FIR Transversal Filter.....	70
5.2.3 Two-Dimensional FIR Filter.....	72
5.3 INFINITE IMPULSE RESPONSE (IIR) FILTERS.....	75
5.3.1 Direct Form IIR Filter.....	75
5.3.2 Cascaded Biquad IIR Filter.....	77
5.4 LATTICE FILTERS	81
5.4.1 All-Zero Lattice Filter.....	81
5.4.2 All-Pole Lattice Filter.....	84
5.5 MULTIRATE FILTERS.....	87
5.5.1 Decimation	88
5.5.1.1 Continuous-Time Sampling.....	88
5.5.1.2 Discrete-Time Sampling.....	89
5.5.1.3 Decimation Filter Structure.....	93
5.5.1.4 ADSP-2100 Decimation Algorithm.....	95
5.5.1.5 A More Efficient Decimator.....	99
5.5.2 Decimator Hardware Configuration.....	102
5.5.3 Interpolation	103
5.5.3.1 Reconstruction of a Discrete-Time Signal.....	104
5.5.3.2 Interpolation Filter Structure.....	107
5.5.3.3 ADSP-2100 Interpolation Algorithm.....	109
5.5.3.4 Interpolator Hardware Configuration.....	113
5.5.4 Rational Sample Rate Changes.....	113
5.5.4.1 L/M Change in Sample Rate.....	114

5.5.4.2	Implementation of Rate Change Algorithm.....	115
5.5.4.3	ADSP-2100 Rational Rate Change Program...	118
5.5.5	Multistage Implementations.....	125
5.5.6	Narrow-Band Spectral Analysis.....	133
5.6	ADAPTIVE FILTERS.....	135
5.6.1	Single-Precision Stochastic Gradient.....	136
5.6.2	Double-Precision Stochastic Gradient.....	138
5.7	REFERENCES	140

CHAPTER 6 ONE-DIMENSIONAL FFTS

6.1	OVERVIEW	141
6.2	RADIX-2 FAST FOURIER TRANSFORMS.....	142
6.2.1	Radix-2 Decimation-In-Time FFT Algorithm.....	142
6.2.2	Radix-2 Decimation-In-Time FFT Program.....	147
6.2.2.1	Main Module.....	147
6.2.2.2	DIT FFT Module.....	148
Butterfly Loop.....	148	
Group Loop.....	155	
Stage Loop.....	156	
DIT FFT Subroutine.....	157	
6.2.3	Radix-2 Decimation-In-Frequency FFT Algorithm.....	160
6.2.4	Radix-2 Decimation-In-Frequency FFT Program.....	166
6.2.4.1	Main Module.....	166
6.2.4.2	DIF FFT Module.....	167
Butterfly Loop.....	167	
Group Loop.....	168	
Stage Loop.....	169	
DIF FFT Subroutine.....	171	
6.2.5	Bit Reversal	173
6.3	BLOCK FLOATING-POINT SCALING.....	178
6.4	OPTIMIZED RADIX-2 DIT FFT.....	181
6.4.1	First Stage Modifications.....	181
6.4.2	Last Stage Modifications.....	183
6.4.3	Optimized Radix-2 DIT FFT Program Listings.....	184
6.5	RADIX-4 FAST FOURIER TRANSFORMS.....	193
6.5.1	Radix-4 Decimation-In-Frequency FFT Algorithm.....	193
6.5.2	Radix-4 Decimation-In-Frequency FFT Program.....	199
6.5.2.1	Main Module.....	199
6.5.2.2	DIF FFT Module.....	200
Butterfly Loop.....	200	
Group Loop.....	204	
Stage Loop.....	205	
Radix-4 DIF FFT Subroutine.....	207	
6.5.3	Digit Reversal.....	213
6.6	OPTIMIZED RADIX-4 DIF FFT.....	215
6.6.1	First Stage Modifications.....	215
6.6.2	Last Stage Modifications.....	216

6.6.3	Program Structure Modifications.....	218	
6.6.4	Data Structure Modifications.....	221	
6.6.4.1	Cosine Table.....	221	
6.6.4.2	In-Place Array.....	221	
6.6.5	Digit-Reversing.....		222
6.6.5.1	Unscrambling Routine.....	223	
6.6.5.2	Modified Butterfly.....	225	
6.6.6	Variations	230	
6.6.6.1	Inverse FFT.....	230	
6.6.6.2	Sizing the Program.....	231	
6.6.7	Programs and File Description.....	231	
6.6.7.1	Twiddle Factors.....	231	
6.6.7.2	Input Data.....	232	
6.6.7.3	FFT Routines.....	232	
6.6.7.4	FFT Program with Unscrambling Routine.....	233	
6.6.7.5	FFT Program with Built-In Digit Reversal.....	234	
6.7	LEAKAGE	244	
6.8	BENCHMARKS		249
6.9	REFERENCES	251	

CHAPTER 7 TWO-DIMENSIONAL FFTS

7.1	TWO-DIMENSIONAL FFTS.....	253	
7.1.1	Row-Column Decomposition.....	254	
7.1.2	Radix-2 FFT	255	
7.1.3	ADSP-2100 Implementation.....	256	
7.1.3.1	Main Module.....	256	
7.1.3.2	Row DIF Module.....	261	
7.1.3.3	Column DIF Module.....	267	
7.1.3.4	Initialization.....	270	
7.1.3.5	Bit Reverse Modules.....	272	
7.1.3.6	Block Floating-Point Adjustment.....	276	
7.2	BENCHMARKS		284

CHAPTER 8 IMAGE PROCESSING

8.1	OVERVIEW		285
8.2	TWO-DIMENSIONAL CONVOLUTION.....	285	
8.3	SINGLE-PRECISION MATRIX MULTIPLY.....	288	
8.4	HISTOGRAM	290	
8.5	REFERENCES	292	

CHAPTER 9 GRAPHICS

9.1	OVERVIEW		293
9.2	GRAPHICS PROCESSING SYSTEM.....	293	

9.3	SETTING THE STAGE.....	295	
9.4	COMPUTATIONAL REDUCTIONS IN TRANSFORMATIONS...	298	
9.5	PROJECTION TECHNIQUES.....	301	
9.6	DATA FORMAT		304
9.7	NORMALIZATION AND SCALING.....	305	
9.8	PROGRAM AND FILE DESCRIPTIONS.....	310	
9.8.1	Object Generation.....	311	
9.8.2	Trigonometric Coefficient Generation.....	316	
9.8.3	FIR Filter Coefficient Generation.....	317	
9.8.4	System Configuration.....	318	
9.8.5	Main Source Program.....	319	
9.8.6	Data Structures.....	321	
9.9	DISPLAY DRIVER	323	
9.10	PERFORMANCE.....		325
9.11	SCHEMATICS.....		328
9.12	SUMMARY		332
9.13	REFERENCES.....		332
9.14	PROGRAM LISTING.....		332

CHAPTER 10 LINEAR PREDICTIVE SPEECH CODING

10.1	OVERVIEW		355
10.2	CORRELATION.....		358
10.3	LEVINSON-DURBIN RECURSION.....	361	
10.4	PITCH DETECTION.....		366
10.5	LINEAR PREDICTIVE CODING SYNTHESIZER.....	370	
10.6	REFERENCES.....		372

CHAPTER 11 PULSE CODE MODULATION

11.1	OVERVIEW		373
11.2	PULSE CODE MODULATION USING μ -LAW.....	374	
11.2.1	μ -Law PCM Encoder.....	374	
11.2.2	μ -Law PCM Decoder.....	376	
11.3	PULSE CODE MODULATION USING A-LAW.....	378	
11.3.1	A-Law PCM Encoder.....	378	
11.3.2	A-Law PCM Decoder.....	380	

CHAPTER 12 ADAPTIVE DIFFERENTIAL PULSE CODE MODULATION

12.1	OVERVIEW		383
12.2	ADPCM ALGORITHM.....		383
12.3	ADPCM ENCODER.....		385
12.3.1	Adaptive Predictor.....	386	
12.3.2	Adaptive Quantizer.....	387	
12.3.3	Inverse Adaptive Quantizer.....	389	

12.3.4	Adaptation Speed Control.....	389	
12.3.5	Predictor Coefficient Update.....	390	
12.3.6	Tone and Transition Detector.....	391	
12.4	ADPCM DECODER.....		392
12.5	NONSTANDARD ADPCM TRANSCODER.....	393	
12.6	COMPANDING TECHNIQUES.....	393	
12.7	BENCHMARKS AND MEMORY REQUIREMENTS.....	396	
12.8	REFERENCES.....		396
12.9	PROGRAM LISTINGS.....		396
12.9.1	Standard ADPCM Transcoder Listing.....	397	
12.9.2	Nonstandard ADPCM Transcoder Listing.....	418	

CHAPTER 13 HIGH-SPEED MODEM ALGORITHMS

13.1	OVERVIEW		433
13.2	SP COMPLEX-VALUED TRANSVERSAL FILTER.....	433	
13.3	COMPLEX-VALUED STOCHASTIC GRADIENT.....	436	
13.4	EUCLIDEAN DISTANCE.....	438	
13.5	REFERENCES.....		440

CHAPTER 14 DUAL-TONE MULTI-FREQUENCY CODING

14.1	INTRODUCTION.....		441
14.2	ADVANTAGES OF DIGITAL IMPLEMENTATION.....	442	
14.3	DTMF STANDARDS.....		443
14.4	DTMF DIGIT GENERATION PROGRAM.....	444	
14.4.1	Digit Entry	449	
14.4.1.1	Key Pad Entry.....	450	
14.4.1.2	Data Memory List.....	451	
14.4.2	Dialing Demonstration.....	453	
14.4.3	Multi-Channel Generation.....	456	
14.5	DECODING DTMF SIGNALS.....	457	
14.5.1	DFTs and FFTs.....	457	
14.5.2	Goertzel Algorithm.....	458	
14.5.2.1	Feedback Phase.....	461	
14.5.2.2	Feedforward Phase.....	461	
14.5.2.3	Choosing N and k.....	463	
14.5.3	DTMF Decoding Program.....	465	
14.5.3.1	Input Scaling.....	466	
14.5.3.2	Multi-Channel DTMF Decoder Software.....	468	
14.5.3.3	Constants, Variables and I/O Ports.....	468	
14.5.3.4	Main Code.....	469	
14.5.3.5	Interrupt Service Routine.....	469	
14.5.3.6	Post-Testing and Digit Validation.....	470	
	Maxrowcol.....	470	
	Minsiglevel.....	471	
	No_Other_Peaks.....	471	

	Twisttests.....	472	
	Check2ndharm.....	472	
	Outputcode.....	473	
	Restart.....	475	
	14.5.3.7 Performance Considerations.....	475	
14.6	REFERENCES.....		477
14.7	PROGRAM LISTINGS.....		478
	14.7.1DTMF Encoder Listing.....	478	
	14.7.2DTMF Decoder Listing.....	484	

CHAPTER 15 SONAR BEAMFORMING

15.1	OVERVIEW		501
15.2	SONAR BEAMFORMING.....	502	
	15.2.1Time-Delay Beamforming.....	503	
	15.2.2Digital Beamforming.....	504	
15.3	DIGITAL BEAMFORMER IMPLEMENTATION.....	508	
	15.3.1Computational Power.....	509	
	15.3.2Memory Usage.....		509
	15.3.3Other Issues	509	
15.4	EXAMPLE BEAMFORMER.....	509	
	15.4.1System Architecture.....	510	
	15.4.2Building Blocks.....		510
	15.4.3System Operation.....	512	
	15.4.4Timing Issues.....		514
	15.4.5Digital Output.....		514
	15.4.6Analog Output.....		515
	15.4.7System Configurations.....	515	
15.5	SYSTEM HARDWARE.....	515	
	15.5.1Component Selection.....	515	
	15.5.2Master Board Hardware.....	517	
	15.5.3Slave Board Hardware.....	520	
	15.5.4A/D Board Hardware.....	522	
15.6	SYSTEM FIRMWARE.....		525
	15.6.1Master Firmware.....	525	
	15.6.2Slave Firmware.....	534	
15.7	SYSTEM SOFTWARE.....	539	
15.8	ENHANCEMENTS.....		540
	15.8.1Additional Features.....	540	
	15.8.2Performance Improvements.....	541	
15.9	REFERENCES.....		543

CHAPTER 16 MEMORY INTERFACE

16.1	OVERVIEW		545
16.2	PROGRAM MEMORY.....		545
	16.2.1Program Memory Bank Enables.....	546	

16.3	DATA MEMORY.....	546
16.3.1	Data Memory Page Enables.....	548
16.3.2	Data Memory Bank Enables.....	549
16.4	I/O CONFIGURATION.....	550
16.4.1	I/O Memory Mapping.....	550
16.4.2	I/O Switches	552

CHAPTER 17 MULTIPROCESSING

17.1	OVERVIEW	553
17.2	SOFTWARE ARCHITECTURE.....	553
17.3	HARDWARE ARCHITECTURE.....	554
17.3.1	Using Dual-Port Memory.....	554
17.3.2	Dual-Port Memory Interface.....	556
17.3.3	Decoder Timing.....	556
17.4	SYNCHRONIZING MULTIPLE ADSP-2100S.....	558
17.5	DEVELOPMENT TOOLS.....	559
17.5.1	System Builder.....	559
17.5.2	Assembler	559
17.5.3	Simulation	563

CHAPTER 18 HOST INTERFACE

18.1	OVERVIEW	565
18.2	INTERFACE CONFIGURATIONS.....	565
18.2.1	Bus Sharing	566
18.2.2	Communication Ports.....	567
18.2.3	Dual-Port Memory.....	568
18.2.4	Memory Swapping.....	569
18.3	ADSP-2100 INTERFACE CONSIDERATIONS.....	569
18.3.1	Bus Request	569
18.3.2	Software Handshake.....	572
18.3.3	Hardware Handshake Using Interrupts.....	572
18.3.4	Software and Hardware Handshake Comparison.....	573
18.4	68000 INTERFACE CONSIDERATIONS.....	573
18.4.1	68000 Addressing.....	573
18.4.2	68000 Bus Signals.....	574
18.5	68000-to-ADSP-2100 BUS SHARING INTERFACE.....	575
18.5.1	Memory Mapping.....	575
18.5.2	Control Registers.....	578
18.5.3	Interprocessor Data Transfers.....	581
18.6	USING PALS.....	582
18.7	680X0 FAMILY OF MICROPROCESSORS.....	584
18.8	SUMMARY	586
18.9	REFERENCES.....	586

INDEX	587
-------------	-----

Preface

This book is about bridging the gap between digital signal processing (DSP) algorithms and their real-world implementations on state-of-the-art digital signal processors. Each chapter tackles a specific application topic, briefly describing the algorithm and discussing its implementation on the ADSP-2100 family of DSP chips.

Anyone who wants to understand how a processor optimized for digital signal processing, such as the ADSP-2100, is used to solve a particular problem will find this book informative. The areas addressed include but are not limited to traditional signal processing, since graphics and numerical applications also benefit from the features of a DSP processor.

We do not attempt to explain the signal processing theory of any application in full detail. Our readers are assumed to already understand the theory and practice applying to their own areas of interest. *Digital Signal Processing in VLSI**, a companion book in the Analog Devices technical reference set, provides much of the necessary basics. The references listed at the end of each chapter provide a wealth of additional information.

This volume spans topics ranging from the very simple to the moderately complex. Here is a brief summary of each section's contents:

- *Fixed-point arithmetic operations*

How basic fixed-point arithmetic operations are mapped onto the hardware of the ADSP-2100.

- *Floating-point arithmetic operations*

How to convert from fixed-point to floating-point representation and vice versa and how to perform basic floating-point arithmetic operations using the ADSP-2100. *Block floating-point* operations are discussed in the chapter on fast Fourier transforms.

- *Function approximations*

How to perform numerical approximations of some useful functions.

- *Digital filters*

Implementations of several finite impulse-response (FIR) and infinite impulse-response (IIR) filters that have fixed coefficients. Also described are multirate

filters, which change the sampling rate of digitally represented signals. This section also discusses adaptive filters (with time-varying coefficients).

- *One-dimensional fast Fourier transforms*

Implementations of several one-dimensional fast Fourier transform (FFT) algorithms and the related operations of bit reversal, digit reversal, block floating-point scaling, and windowing. How to optimize the FFT programs for speed.

- *Two-dimensional fast Fourier transforms*

An implementation of an FFT in two dimensions.

- *Image processing*

Implementations of several algorithms used in processing digitized images.

- *Graphics*

A graphics subsystem based on the ADSP-2100, complete with all software routines and support circuitry.

- *Linear predictive speech coding*

Techniques used to analyze, encode, and synthesize speech signals.

- *Pulse code modulation*

An ADSP-2100 implementation of the CCITT standard pulse-code modulation (PCM) algorithm. Encoding and decoding are shown, employing both μ -law and A-law companding methods.

- *Adaptive differential pulse code modulation (ADPCM)*

An ADSP-2100 implementation of the CCITT standard ADPCM algorithm. A non-standard program that is suitable for some applications is also described.

- *Modem algorithms*

Several algorithms used in implementing high-speed modems.

- *Dual-tone multifrequency coding (DTMF)*

How to generate and detect the CCITT standard DTMF signals.

- *Sonar beamforming*

Both software and hardware for a digital beamforming system for passive sonar.

- *Memory interface*

A design example that shows considerations for implementing an interface between the ADSP-2100 and various types of memory and I/O.

- *Multiprocessing*

An interface between two ADSP-2100s operating in parallel. Dual-port memory and software issues are addressed.

- *Host interface*

How to use the ADSP-2100 as a coprocessor to a host CPU, using the Motorola 68000 as an example.

The text provides comprehensive source-code listings, complete with comments and accompanied by explanatory text. A supplementary diskette—furnished with the book—contains the program listings.

ACKNOWLEDGEMENTS

The substance of this book was contributed by the applications engineers of the Analog Devices DSP Group. They designed, developed and tested the software and the hardware systems presented here, drafted the accompanying documentation and reviewed the final publication. Over time, and with feedback from many customers who put these applications to use, the applications group has also refined much of this information. Besides Bob Fine, who heads the group, contributors include: Dan Ash, Chris Caviglioli, Ron Coughlin, Steve Cox, Jeff Cuthbert, Fares Eidi, Cole Erskine, Hayley Greenberg, Matt Johnson, Kapriel Karagozyan, Gerald McGuire, Gordon Sterling and Bruce Wolfeld.

Jim McQuaid provided significant editorial feedback on all chapters; Adele Hastings produced virtually all drawings and layout; Sandra Perry and other Marketing engineers gave comments and input.

Amy Mar

Norwood, Mass.

* **Higgins, Richard J. 1990.** *Digital Signal Processing in VLSI.* Englewood Cliffs, NJ: Prentice-Hall.